hole, on a portion of the fourth barrier layer between the trench and via hole, and at a bottom of the via hole;

etching to remove the sixth barrier layer from, and stopping on, the fifth barrier layer, from and stopping on the fourth barrier layer, and at the bottom of the via hole, leaving a portion of the sixth barrier layer as a liner on the side surfaces of the third dielectric layer defining the trench and on the side surfaces of the second dielectric layer defining the via hole; and

filling the dual damascene opening with metal to form a metal line connected to an underlying metal via.

Please add new claim 21.

21. (New) The method according to claim 1, comprising etching to form the first opening having entire side surfaces which are substantially parallel.

REMARKS

Claims 1 through 21 are pending in this application, of which claims 13 through 20 stand withdrawn from consideration pursuant to the provisions of 37 C.F.R.§1.42(b). Claims 6 through 12 have been indicated allowable. Accordingly, the only substantive issue pivots about the patentability of claims 1 through 5 and 21.

Claims 1 and 6 have been amended and claim 21 added. Care has been exercised to avoid the introduction of new matter. Claim 6 has been placed in independent form. Amended claim 1 and new claim 21 find adequate descriptive support throughout the originally filed disclosure as, for example, Fig. 3 and the related discussion thereof in the

written description of the specification. Applicants submit that the present Amendment does not generate any new matter issue.

A clean copy of amended claims 1 and 6, and of new claim 21, appear in the Appendix hereto.

Objection the Specification

The Examiner required a new specification with appropriate margins. In response Applicants submit herewith as Exhibit A, a copy of the originally filed specification with appropriate margins. No amendment has been made to the specification.

Claims 1, 2, 4 and 5 were rejected under 35 U.S.C. §102 for lack of novelty as evidenced by Chooi et al.

In the statement of the rejection, the Examiner referred to Figs. 1 and 4 through 8, and to related portions of the text, asserting the disclosure of a method identically corresponding to that claimed. This rejection is traversed.

The factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of a claimed invention, such that the identically claimed invention is placed into the recognized possession of one having ordinary skill in the art. *Crown Operations International Ltd. v. Solutia, Inc., 289 F.3d 1367 62 USPQ2d 1917(Fed. Cir. 2002); Helifix Ltd. v. Blok-Lok, Ltd. 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); Electro Medical Systems S.A. v. Cooper Life Sciences, Inc., 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).* There is a significant difference between the method defined in independent claim 1 and the methodology of Chooi et al.

that scotch the factual determination that Chooi et al. identically describe the claimed invention within the meaning of 35 U.S.C. §102.

Specifically, independent claim 1, as best appreciated from Fig. 3, is directed to a method comprising a sequence of manipulative steps, including forming a **single** dielectric layer (30) over a substrate, and then forming a first barrier layer 31 thereon with an interface therebetween. No such methodology is disclosed or suggested by Chooi et al. Rather, Chooi et al. disclose a dual damascene technique wherein, as recognized by the Examiner, four layers, i.e., layers 12, 14, 16 and 18 (although layer 16 is optional) are formed over a substrate all of which have been cumulative identified by the Examiner as the first dielectric layer. However, in accordance with the present invention, a single layer is deposited as the first dielectric layer.

The above argued difference between the claimed method and the methodology of Chooi et al. is not mere semantics. It is apparent that Chooi et al. employ different dielectric layers to form a dual damascene structure; whereas, the opening defined by the methodology of the invention set forth in independent claim 1 as a single damascene opening, i.e., a trench.

The above argued functionally significant difference between the method defined in independent claim 1 and the methodology of Chooi et al. undermines the factual determination that Chooi et al. identically describe the claimed invention within the meaning of 35 U.S.C. §102. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc., 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986).* Applicants therefore, submit that the imposed rejection of claims 1, 2, 4 and 5 under 35

U.S.C. §102 for lack of novelty as evidenced by Chooi et al. is not factually viable and, hence, solicit withdrawal thereof.

Claim 3 was rejected under 35 U.S.C. §103 for obviousness predicated upon Chooi et al. in view of Chung et al.

This rejection is traversed. Specifically, claim 3 depends from independent claim 1. Applicants incorporate herein the arguments previously advanced in traversing the imposed rejection of claim 1 under 35 U.S.C. §102 for lack of novelty as evidenced by Chooi et al. Indeed, Chooi et al. neither disclose nor suggest forming an opening in a single first dielectric layer overlying the substrate. The additional reference to Chung et al. does not cure the argued deficiencies of Chooi et al. Ergo, even if the applied references are combined, the claimed invention would not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).*

Applicants, therefore, submit that the imposed rejection of claim 3 under 35 U.S.C. §103 for obviousness predicated upon Chooi et al. in view of Chung et al. is not factually or legally viable and, hence, solicit withdrawal thereof.

New Claim 21

New claim 21 is free of the applied prior art by virtue of its dependence of independent claim 1, the patentability of which has been argued supra. Moreover, Applicants separately argue the patentability of claim 21 which specifies that the entire side surfaces of the first opening are substantially parallel, noting Fig. 3 with side surfaces 30A. On the other hand, the opening identified by the Examiner in Chooi et al.

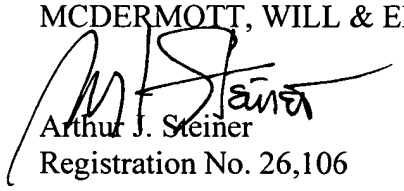
is a dual damascene opening wherein the entire side surfaces of the opening are not parallel.

It should, therefore, be apparent that the objection and rejections have been overcome and that all active claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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APPENDIX

Claims 1 and 6 now read as follows.

1. (Amended) A method of manufacturing a semiconductor device, the method comprising:

B1

forming a single first dielectric layer overlying a substrate;

forming a first barrier layer, comprising a first dielectric barrier material, on the single first dielectric layer with an interface therebetween,

etching to form a first opening defined by side surfaces of the first dielectric layer and a bottom;

forming a second barrier layer, comprising a second dielectric barrier material different from the first dielectric barrier material, on an upper surface of the first barrier layer overlying the single first dielectric layer, on the side surfaces of the single first dielectric layer defining the first opening and on the bottom of the opening;

etching, with selectivity to the first barrier layer, to remove the second barrier layer from, and stopping on, the upper surface of the first barrier layer, and to remove the second barrier layer from the bottom of the first opening, leaving a portion of the second barrier layer as a liner on the side surfaces of the first dielectric layer defining the first opening; and

filling the opening with metal to form a lower metal feature.

6. (Amended) A method of manufacturing a semiconductor device, the

B2

method comprising:

forming a first dielectric layer overlying a substrate;

forming a first barrier layer, comprising a first dielectric barrier material, on the first dielectric layer;

etching to form a first opening defined by side surfaces of the first dielectric layer and a bottom;

forming a second barrier layer, comprising a second dielectric barrier material different from the first dielectric barrier material, on an upper surface of the first barrier layer overlying the first dielectric layer, on the side surfaces of the first dielectric layer defining the first opening and on the bottom of the opening;

B2 cont.

etching, with selectivity to the first barrier layer, to remove the second barrier layer from, and stopping on, the upper surface of the first barrier layer, and to remove the second barrier layer from the bottom of the first opening, leaving a portion of the second barrier layer as a liner on the side surfaces of the first dielectric layer defining the first opening;

filling the opening with metal to form a lower metal feature;

forming a third barrier layer, comprising a third dielectric barrier material different from the first dielectric barrier material, on the first barrier layer and on an upper surface of the lower metal feature;

forming a second dielectric layer on the third barrier layer;

forming a fourth barrier layer, comprising a fourth dielectric barrier material, on the second dielectric layer;

forming a third dielectric layer on the fourth barrier layer;

forming a fifth barrier layer, comprising a fifth dielectric barrier material, on the third dielectric layer;

etching to form a dual damascene opening comprising an upper trench portion defined by side surfaces of the third dielectric layer in communication with a lower via hole defined by side surfaces of the second dielectric layer and a bottom on at least a portion of the upper surface of the lower metal feature;

forming a sixth barrier layer, comprising a sixth dielectric barrier material different from the first, fourth and fifth dielectric materials, on the fifth barrier layer overlying the third dielectric layer, on the side surfaces of the third dielectric layer defining the trench, on the side surfaces of the second dielectric layer defining the via hole, on a portion of the fourth barrier layer between the trench and via hole, and at a bottom of the via hole;

B2

etching to remove the sixth barrier layer from, and stopping on, the fifth barrier layer, from and stopping on the fourth barrier layer, and at the bottom of the via hole, leaving a portion of the sixth barrier layer as a liner on the side surfaces of the third dielectric layer defining the trench and on the side surfaces of the second dielectric layer defining the via hole; and

filling the dual damascene opening with metal to form a metal line connected to an underlying metal via.

New claim 21 read as follow.

B3

21. (New) The method according to claim 1, comprising etching to form the first opening having entire side surfaces which are substantially parallel.